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Asymmetrical DC-Sourced Multilevel Inverter with Reduced Switching Components

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ABSTRACT: Recent advancements in the field of power electronics have created an effective platform for exploring various multilevel inverter (MLI) topologies. These topologies exhibit several significant features, including high-quality staircase sinusoidal output voltage, reduced power switch count, and elimination of output filters. In this study, a novel asymmetrical multilevel inverter topology is proposed with the objective of minimizing the number of inverter components while achieving efficient voltage step generation. The proposed MLI configuration produces a high-step, staircase-like output waveform that closely approximates a sinusoidal voltage without increasing the number of power semiconductor switches. A carrier-based Sinusoidal Pulse Width Modulation (CB-PWM) technique operating at a switching frequency of 3 kHz is utilized for control. The operating principle of the proposed inverter is explained in detail. A 27-level inverter configuration is modeled and simulated in the MATLAB/Simulink R2019b environment to analyze its performance with an RL load under different modulation indices. Furthermore, A comparative analysis is conducted between the proposed topology and existing multilevel inverter configurations to evaluate its performance.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained significant importance in power electronic converters due to their wide range of applications and inherent advantages [1], [2]. With the continuously increasing demand for electrical power, the integration of MLIs with modern power electronic systems has become essential [3]. MLIs are extensively used in variable-frequency drives, electric vehicles, and high-voltage DC (HVDC) transmission systems [4], [5]. In addition, they play a vital role in renewable energy conversion systems, including solar and wind energy applications [6], [7]. MLIs are particularly suitable for medium-voltage and high-power applications [8]. In MLIs, higher output voltage levels are synthesized in a staircase waveform by combining multiple DC sources. This stepped output closely approximates a sinusoidal waveform, thereby reducing total harmonic distortion (THD) [9]. As a result, the requirement for output filters is significantly minimized [10]. Furthermore, the staircase nature of the output reduces the dv/dt stress across switching devices [11]. Since the voltage stress across individual switches is lower, devices with lower voltage ratings can be employed, making the system more cost-effective [12]. Many multilevel topologies also offer redundant switching states, which can be utilized to implement fault-tolerant operation [13]. The three classical MLI topologies introduced over time are the Neutral Point Clamped (NPC) inverter [14], the Flying Capacitor (FC) inverter [15], and the Cascaded H-Bridge (CHB) inverter [16]. Although these conventional topologies provide substantial advantages over traditional two-level inverters, they suffer from certain drawbacks such as a high number of switches, multiple DC sources, and numerous capacitors [17]. To overcome these limitations, several new MLI topologies have been developed aiming to reduce component count and improve efficiency [18]–[20]. These modern configurations are broadly classified into symmetrical and asymmetrical types based on the magnitude of their DC voltage sources [21]. In symmetrical MLIs, all DC sources have equal voltage levels, whereas in asymmetrical MLIs, the DC source magnitudes differ [22]. Various modulation techniques have been proposed for MLIs, including Selective Harmonic Elimination (SHE) [23], Space Vector Pulse Width Modulation (SVPWM) [24], Carrier-Based Pulse Width Modulation (CB-PWM) [25], and Nearest Level Control (NLC) [26]. Several studies also discuss the use of H-bridge configurations to generate positive and negative voltage polarities [16], [27]. Moreover, some reported topologies require a greater number of DC sources than power switches, which increases system complexity [28]. In this paper, an asymmetrical 27-level MLI is proposed. The performance of the proposed topology is evaluated using MATLAB/Simulink simulations for RL-load in different modulation indices. A comparative analysis with recent MLI topologies is also presented. The paper is organized as follows: Section 3 explains the switching pulse generation and detailed operating modes of the proposed circuit. Section 4 presents a Modes of operation. Section 5 discusses the simulation parameters and performance results.

II. PROPOSED CIRCUIT TOPOLOGY

The proposed inverter configuration, depicted in Fig.1, is composed of thirteen power semiconductor switches labelled S_1 through S_{13} . Among these, S_2 is designed as a bidirectional switch capable of four-quadrant operation, allowing current flow in both directions with voltage blocking capability in both polarities. The remaining twelve switches are unidirectional and operate in two quadrants. The topology utilizes four isolated DC voltage sources: V_1 , V_2 , V_3 , and V_4 . These sources are arranged asymmetrically, meaning their voltage magnitudes are intentionally different rather than equal. This unequal voltage configuration enables the inverter to generate a larger number of output voltage levels with fewer components. When the DC sources are selected as $V_1 = 5V_{dc}$, $V_2 = 5V_{dc}$, $V_3 = V_{dc}$, $V_4 = 3V_{dc}$, the proposed multilevel inverter is capable of producing a 27-level stepped output voltage waveform, which closely approximates a sinusoidal signal.

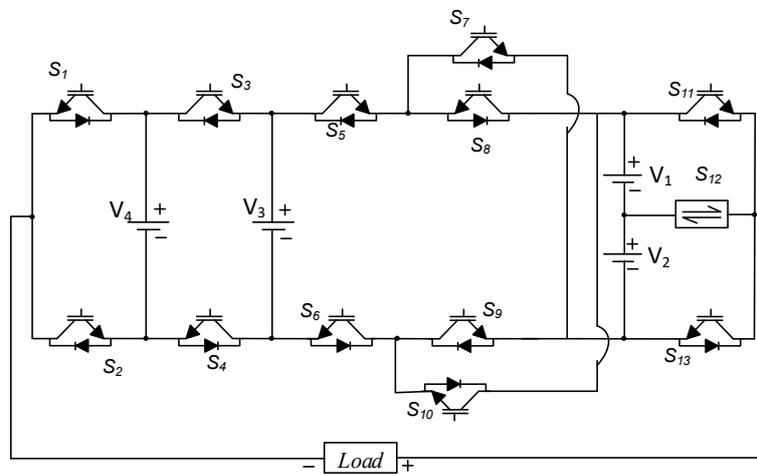
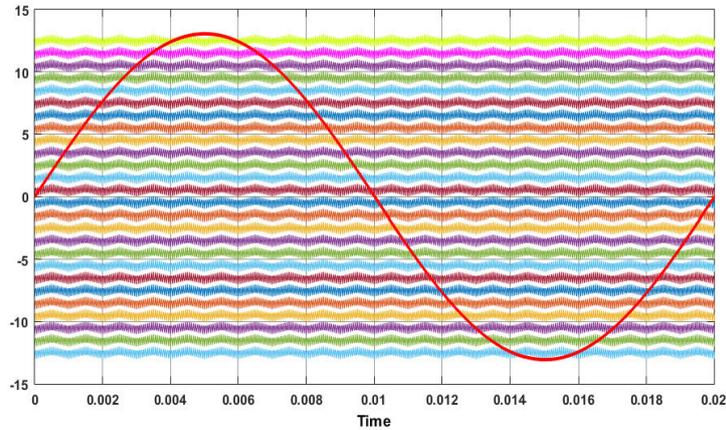


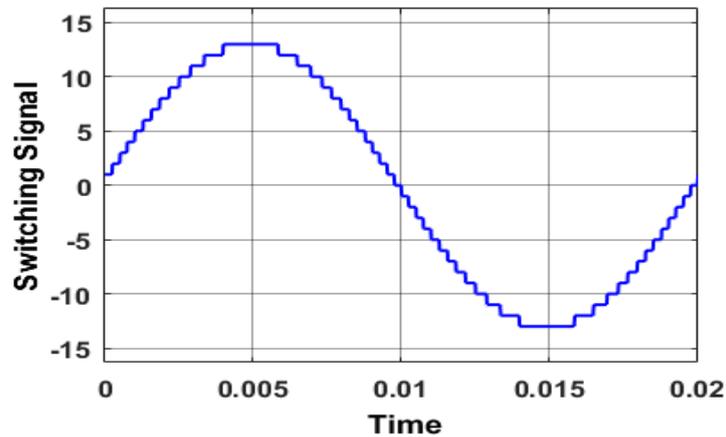
Fig. 1. Proposed MLI topology

III. MODES OF OPERATION

MLI employ a large number of power switches to generate a stepped output voltage waveform. The staircase nature of the output is achieved by appropriately controlling these switches using suitable modulation strategies. As discussed earlier, several modulation techniques have been developed for MLIs. In this work, the Sinusoidal Pulse Width Modulation (SPWM) technique is adopted. For the 27-level inverter, twenty-six triangular carrier signals are used to generate the required PWM signals, as illustrated in Fig. 2(a). These carrier waveforms are continuously compared with a single sinusoidal reference signal through twenty-six comparators. Each comparator produces a digital output based on the comparison between the reference and its corresponding carrier signal. The outputs from all twenty-six comparators are then logically combined to form a composite switching signal, as shown in Fig. 2(b). The real-time simulation waveform of this switching signal for the single-phase 27-level inverter is also presented in Fig. 2(b). Finally, this combined switching signal is decoded according to the switching states listed in Table 1 to generate the appropriate gate pulses for the individual switches of the proposed inverter topology. For each voltage level, the ON and OFF states of all thirteen switches are clearly defined. These switching states determine how the isolated DC sources are combined to obtain the required stepped output voltage. The detailed explanation of these switching combinations ensures a clear understanding of the operation of the proposed 27-level inverter in both positive and negative half-cycles.



(a)



(b)

Fig.2: PWM generation: (a) Comparison of carriers with reference signal; (b) Corresponding switching signal of the 27-MLI.

The generation of different voltage levels in the proposed 27-level inverter is achieved by properly selecting specific combinations of switches in each operating mode. For the maximum positive voltage level, +13Vdc, switches S11, S10, S5, S3, and S2 are turned ON, whereas the corresponding minimum negative voltage level, -13Vdc, is obtained by activating S11, S8, S10, S6, and S2. Similarly, +12Vdc is produced by turning ON S11, S9, S6, S3, and S2, while -12Vdc is generated using S13, S8, S5, S4, and S1. For the +11Vdc level, switches S11, S10, S5, S4, and S2 conduct, whereas -11Vdc is achieved through S13, S7, S6, S3, and S1. The +10Vdc and -10Vdc levels are obtained by activating S11, S9, S6, S4, and S2, and S13, S8, S5, S3, and S1, respectively. In a similar manner, +9Vdc is produced using S11, S9, S6, S3, and S1, while -9Vdc is achieved by turning ON S13, S8, S5, S4, and S2. For the intermediate voltage levels, +8Vdc is generated by switches S12, S10, S5, S3, and S2, whereas -8Vdc is obtained through S13, S7, S6, S3, and S2. The +7Vdc and -7Vdc levels are formed using S12, S9, S6, S3, and S2, and S13, S8, S5, S3, and S2, respectively. Similarly, +6Vdc is achieved with S12, S10, S5, S4, and S2, while -6Vdc is produced using S12, S7, S6, S3, and S1. Further reduction in voltage levels follows the same principle of controlled switching. The +5Vdc and -5Vdc levels are generated through the combinations S12, S9, S6, S4, S2 and S12, S8, S5, S3, S1, respectively. For +4Vdc and -4Vdc, the required switch combinations are S12, S9, S6, S3, S1 and S12, S8, S5, S4, S2. The +3Vdc level is obtained by turning ON S11, S8, S5, S3, and S2, while -3Vdc is produced using S13, S9, S6, S4, and S1. Likewise, +2Vdc is generated with S13, S9, S6, S3, and S2, and -2Vdc with S13, S10, S5, S4, and S1. The +Vdc level is achieved by activating S13, S10, S5, S4, and S2, whereas -Vdc is produced when S13, S10, S5, S4, and S1 are turned ON. Finally, the zero-voltage level is obtained by switching ON S13, S9, S6, S3, and S1. Overall, each voltage level—both positive and negative—is realized through a unique combination of five conducting switches, ensuring proper connection of the asymmetric DC sources to synthesize the desired stepped output waveform. The switching states of

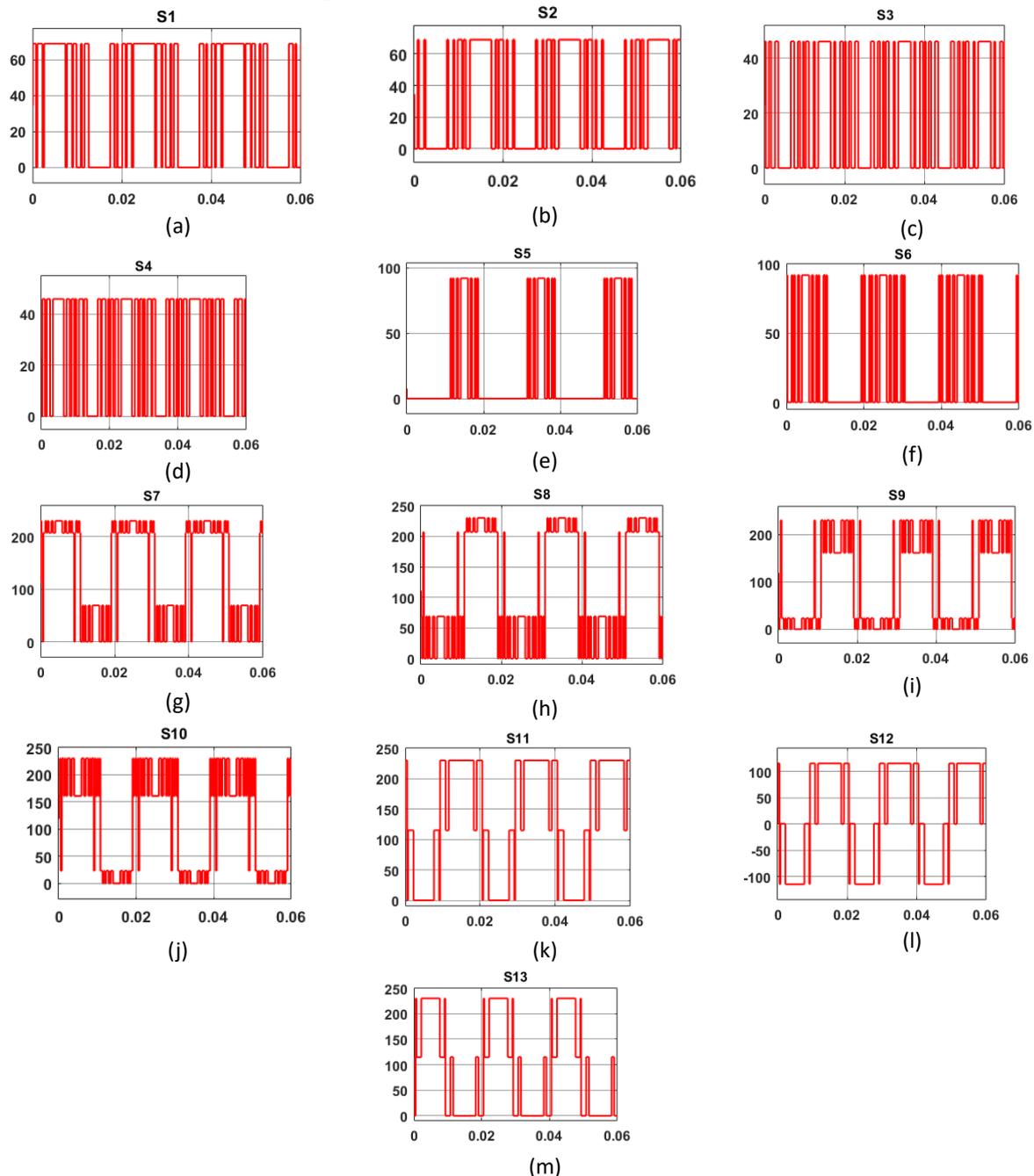
the proposed multilevel inverter (MLI) are presented in Table. 1. In the table, the operating condition of each switch is indicated using specific symbols. A green check mark (√) represents that the corresponding switch is in the ON state, allowing current to flow through it. On the other hand, a red cross (×) denotes that the switch is in the OFF state, blocking the current path. This representation clearly illustrates the switching combinations required to generate the different output voltage levels of the inverter.

Table. 1 Switching states of proposed 27-level MLI.

	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃
+13V _{dc}	×	√	√	×	√	×	×	×	×	√	√	×	×
+12V _{dc}	√	√	√	×	×	√	×	×	√	×	√	×	×
+11V _{dc}	×	√	×	√	√	×	×	×	×	√	√	×	×
+10V _{dc}	×	√	×	√	×	√	×	×	√	×	√	×	×
+9V _{dc}	√	×	×	×	×	√	×	×	√	×	√	×	×
+8V _{dc}	×	√	√	×	√	×	×	×	×	√	×	√	×
+7V _{dc}	×	√	√	×	×	√	×	×	√	×	×	√	×
+6V _{dc}	×	√	×	√	√	×	×	×	×	√	×	√	×
+5V _{dc}	×	√	×	√	×	√	×	×	√	×	×	√	×
+4V _{dc}	√	×	×	×	×	√	×	×	√	×	×	√	×
+3V _{dc}	×	√	√	×	√	×	×	√	×	×	√	×	×
+2V _{dc}	×	√	√	×	×	√	×	×	√	×	×	×	√
+1V _{dc}	×	√	×	√	√	×	×	×	×	√	×	×	√
0V _{dc}	√	×	×	×	×	√	×	×	√	×	×	×	√
-1V _{dc}	√	×	×	√	√	×	×	×	×	√	×	×	√
-2V _{dc}	√	×	×	√	√	×	×	×	×	√	×	×	√
-3V _{dc}	√	×	×	√	×	√	×	×	√	×	×	×	√
-4V _{dc}	×	√	×	√	√	×	×	√	×	×	×	√	×
-5V _{dc}	√	×	×	×	√	×	×	√	×	×	×	√	×
-6V _{dc}	√	×	×	×	×	√	√	×	×	×	×	√	×
-7V _{dc}	×	√	√	×	√	×	×	√	×	×	×	×	√
-8V _{dc}	×	√	√	×	×	√	√	×	×	×	×	×	√
-9V _{dc}	×	√	×	√	√	×	×	√	×	×	×	×	√
-10V _{dc}	√	×	√	×	√	×	×	√	×	×	×	×	√
-11V _{dc}	√	×	√	×	×	√	√	×	×	×	×	×	√
-12V _{dc}	√	×	×	√	√	×	×	√	×	×	×	×	√
-13V _{dc}	×	√	×	×	×	√	×	√	×	√	√	×	×

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the simulation results of the proposed 27-level inverter have been discussed. In MLIs, the term “blocking voltage” signifies the voltage threshold that every switching component, IGBTs or MOSFETs, must endure while in the inactive state. Surpassing the threshold can trigger the semiconductor breakdown, resulting in malfunction and potentially harming the entirety of the inverter system. Therefore, selecting switching devices with appropriate voltage ratings is crucial in multilevel inverter design to ensure reliability and safe operation. The blocking voltages across switches are depicted below in Fig. 2. The value of the blocking voltage across the switches S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12 and S13 are 65 V, 65 V, 45 V, 45 V, 90 V, 90 V, 225 V, 225 V, 225 V, 225 V, 225 V, 110 V and 225 V respectively as shown in Fig. 2. All measured blocking voltages are within the IGBT’s rated capacity, confirming the safe and reliable operation of the proposed inverter topologies.



This section presents the simulation analysis of the proposed 27-level MLI. The model is developed and simulated using MATLAB/Simulink to evaluate the performance of the topology under specified operating conditions. For the proposed configuration, the DC source magnitudes are selected as $V_1 = 150$ V, $V_2 = 150$ V, $V_3 = 30$ V, and $V_4 = 90$ V. This unequal selection of source magnitudes ensures asymmetrical operation and enables the generation of 27 output voltage levels. The performance of the inverter is analysed at different values of modulation index 1 and 0.6. Figure 5 shows the simulation results at a modulation index of 1. The inverter is tested with an RL load having resistance $R = 100$ ohm and inductance $L = 80$ mH. The input DC voltage is chosen as $V_{dc} = 30$ V, which gives $3V_{dc} = 90$ V and $5V_{dc} = 150$ V for the respective sources. Under these operating conditions, the maximum output voltage obtained from the simulation is 390 V, as shown in Fig. 5(a), while the corresponding maximum load current is 3.8 A, as illustrated in Fig. 5(b). The total harmonic distortion (THD) of the output voltage for this configuration is 4.24%, as presented in Fig. 5(c). These results confirm that the proposed inverter is capable of producing a multi-step output waveform with acceptable harmonic performance at the selected modulation index 1.

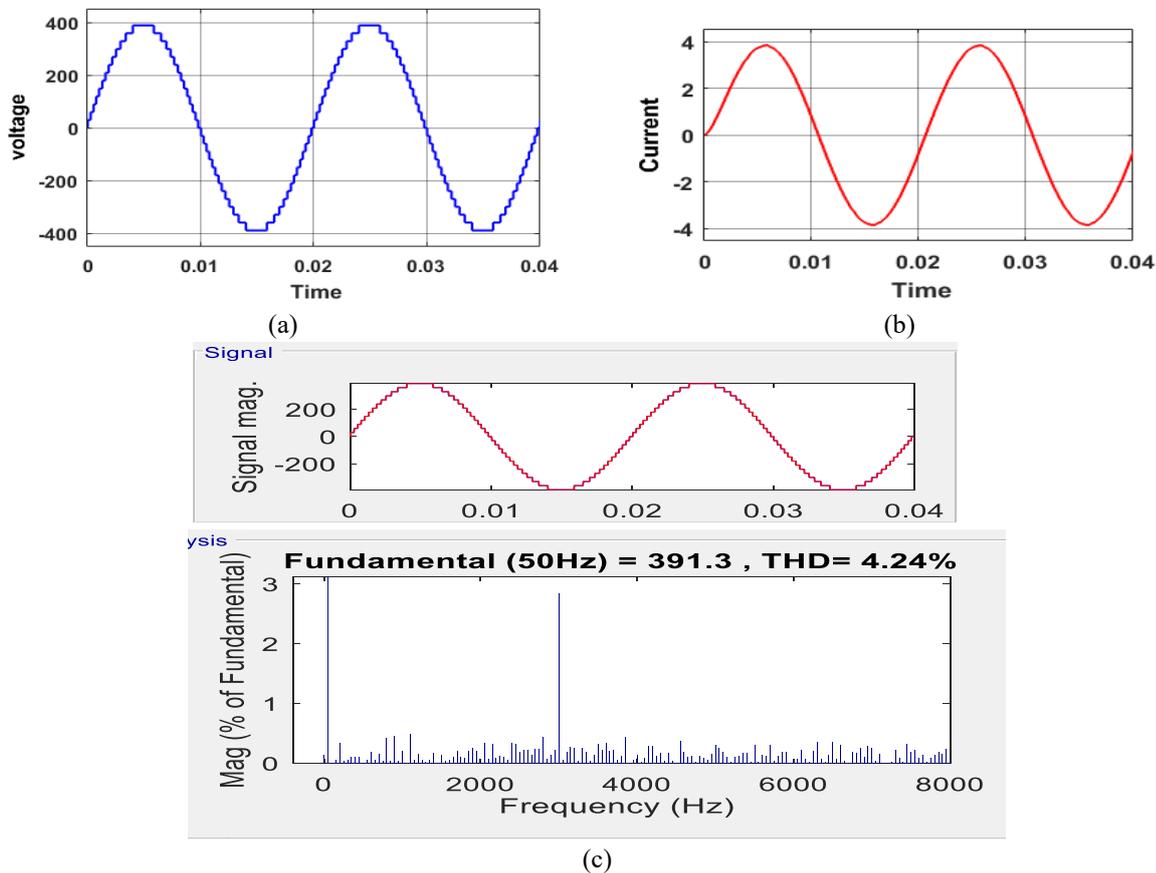


Fig. 5 Simulation results for the (a) Output Voltage (b) Load Current (c) Total Harmonic Distortion of the output voltage at modulation index 1.

Using the same load parameters and input voltage conditions, the performance of the proposed 27-level inverter is further evaluated at a modulation index of 0.6. The corresponding simulation results are presented in Fig. 6. At a modulation index of 0.6, the maximum output voltage obtained from the simulation is 240 V, as shown in Fig. 6(a). The corresponding maximum load current is 2.35 A, as illustrated in Fig. 6(b). These results indicate that increasing the modulation index significantly improves the output voltage magnitude thereby enhancing the overall performance of the proposed 27-level inverter.

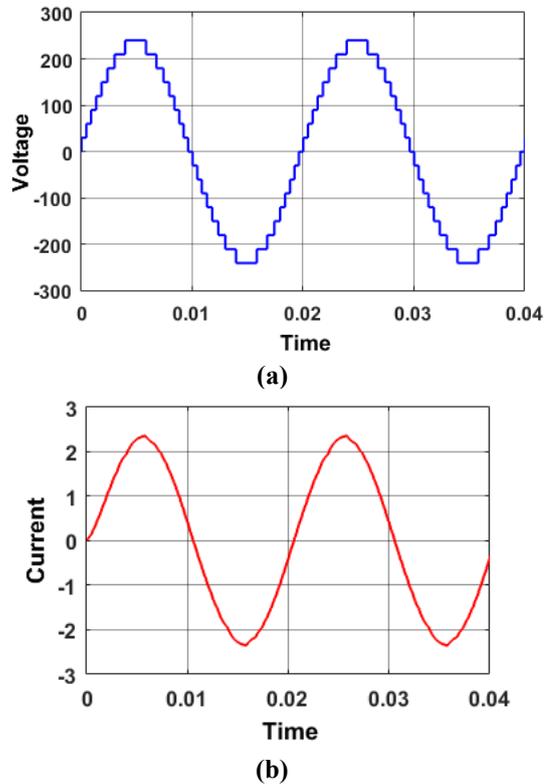


Fig. 6 Simulation results for the (a) Output Voltage (b) Load Current at modulation index 0.6.

V. CONCLUSION

This paper presented a novel 27-level multilevel inverter topology capable of generating a high-quality output voltage waveform with reduced harmonic distortion. The proposed configuration effectively utilizes asymmetrical DC sources to achieve multiple voltage levels while maintaining satisfactory performance under different modulation indices. The simulation results demonstrate that the inverter produces a near-sinusoidal output with significantly improved THD at higher modulation indices, confirming the effectiveness of the control strategy and topology. In addition to its present advantages, the proposed topology offers promising scope for further enhancement. Future work can focus on reducing the number of DC voltage sources and minimizing the variation among source magnitudes without compromising the number of output levels. Such optimization would simplify the circuit structure, reduce component count, and lower system cost. Moreover, the topology can be further adapted for photovoltaic (PV) applications by configuring it to operate with fewer DC sources derived directly from PV arrays. This modification would help reduce the blocking voltage across switches and decrease the total standing voltage, thereby lowering switching stress and improving overall efficiency and reliability. With these potential improvements, the proposed inverter can serve as a competitive and scalable solution for medium- and high-power renewable energy applications.

REFERENCES

1. Lai, J. S., & Peng, F. Z. (2002). Multilevel converters—A new breed of power converters. *IEEE Transactions on Industry Applications*, 38(3), 509-517.
2. Rodriguez, J., et al. (2002). Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics*, 49(4), 724-738.
3. Kouro, S., et al. (2010). Recent advances and future trends in multilevel power conversion. *IEEE Transactions on Industrial Electronics*, 57(7), 2553-2570.

4. Steinke, J. K. (1999). Use of self-commutated inverters in electric drive systems and line-side converters. *IEEE Transactions on Industry Applications*, 35(1), 88-95.
5. Lesnicar, A., & Marquardt, R. (2003). An innovative modular multilevel converter topology suitable for a wide power range. *IEEE Power Tech Conference*.
6. Saeedifard, M., & Iravani, R. (2010). Dynamic performance of a modular multilevel back-to-back HVDC system. *IEEE Transactions on Power Delivery*, 25(4), 2903-2912.
7. Blaabjerg, F., et al. (2006). Power electronics as efficient interface in dispersed power generation systems. *IEEE Transactions on Power Electronics*, 21(5), 1193-1208.
8. Toliyat, H. A., et al. (2003). A review of multilevel power conversion topologies for high-power applications. *IEEE Transactions on Power Electronics*, 18(1), 1-15.
9. McGrath, B. P., & Holmes, D. G. (2002). Multicarrier PWM strategies for multilevel inverters. *IEEE Transactions on Industrial Electronics*, 49(4), 858-867.
10. Corzine, K. A., et al. (2004). Control of cascaded multilevel inverters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 51(10), 2039-2049.
11. Kouro, S., et al. (2007). Reduced switching-frequency active-front-end multilevel inverter with improved power quality. *IEEE Transactions on Industrial Electronics*, 54(6), 3055-3063.
12. Busse, D., et al. (1997). Bearing currents and their relationship to PWM drives. *IEEE Transactions on Power Electronics*, 12(2), 243-252.
13. Pou, J., et al. (2005). Fault-tolerant operation of the neutral-point-clamped inverter. *IEEE Transactions on Industrial Electronics*, 52(2), 444-452.
14. Nabae, A., et al. (1981). A new neutral-point-clamped PWM inverter. *IEEE Transactions on Industry Applications*, IA-17(5), 518-523.
15. Meynard, T. A., & Foch, H. (1992). Multi-level conversion: Multi-level DC voltage step conversion. *IEEE Power Electronics Specialists Conference (PESC)*, 131-138.
16. Lai, J. S., & Peng, F. Z. (1996). Multilevel converters: A new breed of power converters. *IEEE Industry Applications Society Annual Meeting*.
17. Rodriguez, J., et al. (2009). Multilevel converters: An enabling technology for high-power applications. *Proceedings of the IEEE*, 97(11), 1786-1817.
18. Gupta, K. K., & Jain, S. (2014). Comprehensive review of a recently proposed multilevel inverter. *IET Power Electronics*, 7(3), 467-479.
19. Babaei, E., & Hosseini, S. H. (2009). New cascaded multilevel inverter topology with minimum number of switches. *Energy Conversion and Management*, 50(11), 2761-2767.
20. Ekanayake, J. B., et al. (2012). A review of multilevel inverter topologies for renewable energy applications. *IEEE Transactions on Sustainable Energy*.
21. Franquelo, L. G., et al. (2008). The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine*, 2(2), 28-39.
22. Nabae, A., et al. (1981). (See [14] - foundational for source magnitude analysis). Note: Newer papers often cite [22] as the specific comparison of asymmetrical vs. symmetrical source sizing.
23. Patel, H. S., & Hoft, R. G. (1973). Generalized techniques of harmonic elimination and voltage control in thyristor inverters. *IEEE Transactions on Industry Applications*, 9(3), 310-317.
24. Holtz, J. (1992). Pulsewidth modulation—A survey. *IEEE Transactions on Industrial Electronics*, 39(5), 410-420.
25. Carrara, G., et al. (1992). A new multilevel PWM method: A theoretical analysis. *IEEE Transactions on Power Electronics*, 7(3), 497-505.
26. Veenstra, M., & Rufer, A. (2005). PWM modulation method for a five-level converter. *IEEE Transactions on Power Electronics*, 20(3), 575-583.
27. Leon, J. I., et al. (2011). Multilevel voltage source inverter topologies for grid-connected photovoltaic systems. *IEEE Transactions on Industrial Electronics*, 58(8), 3500-3507.
28. Khazraei, M., et al. (2012). A modular current-source multilevel inverter. *IEEE Transactions on Power Electronics*, 27(12), 4811-4819



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